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HIGH FREQUENCY POWER AMPLIFIER

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a high frequency power amplifier, and more specifically, to a high frequency power amplifier used in microwave or millimetric-wave telecommunications equipment for mobile communications or satellite communications.

Description of Related Art

In conventional high frequency power amplifiers used in microwave or millimetric-wave telecommunications equipment for mobile communications or satellite communications, it is well known that the efficiency of transistor operation is higher if the load at the frequencies of not only the fundamental waves but also higher harmonics of the output circuit of a transistor is controlled, as compared with the case where only the load of fundamental waves is controlled. Here, the fundamental waves are the waves that have the lowest frequency, and the higher harmonics are a series of waves, each of which has a frequency that is an integral multiple of the fundamental frequency.

It has been reported that there are the optimal load conditions for high-efficiency operation in input high frequency loads. For example, Japanese Patent No. 2695395 titled "High Frequency Power Amplifier" discloses that the control of input-side higher harmonics is effective for improving a drain efficiency; the input-side higher harmonic control circuit has a resonance frequency with respect to frequencies lower than the frequency of the 2nd harmonic; there are optimal load conditions in the input impedance range of $(0 + j4 \Omega)$, $(0 + j25 \Omega)$, $(5 + j25 \Omega)$, and $(5 + j4 \Omega)$; and the efficiency of operation can be higher when the impedance of the 2nd harmonic is set in a low range. Here, higher harmonics, each of which has a frequency that is an odd-number multiple of the fundamental frequency, are called odd number order higher harmonics; and higher harmonics, each of which has a frequency that is an even-number

multiple of the fundamental frequency, are called even number order higher harmonics.

Japanese Patent Laid-Open No. 7-22872 titled Electric Power Amplifier discloses that it is effective to make the load condition of input/output higher harmonics a short-circuit load in order to achieve high-efficiency operation in a hetero-junction bipolar transistor, and that, as in the above-described Japanese Patent No. 2695395, the efficiency of the transistor can be improved by setting a low impedance load. It is disclosed that there is no or little effect of odd number order higher harmonics, in particular of a 3rd higher harmonic.

As described above, conventional circuit configurations for realizing the high efficiency of the operation of transistors in a high frequency power amplifier have a problem in that the circuit configurations are limited to make the input-side even-number-order higher harmonic load of the impedance matching circuit a short-circuit load.

Furthermore, such a high frequency power amplifier have a problem in that the higher the frequency of a signal, that is the higher the order of higher harmonics, the smaller the amplitude of the higher harmonics reflected from the higher harmonic processing circuit until the higher harmonics reach the input end of the transistor due to propagation loss in a line, and sufficient reflection cannot be obtained.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to solve the above-described problems, and to provide a high frequency power amplifier that can improve the efficiency of transistor operation without limiting the input-side higher harmonic load of an impedance matching circuit to a short-circuit load.

Another object of the present invention is to provide a high frequency power amplifier that can increase the quantity of the reflection of higher harmonics.

According to a first aspect of the present invention, there is provided a high frequency power amplifier, comprising: a transistor for amplifying signals; and an input-side impedance matching circuit connected to an input side of the

transistor, wherein the input-side impedance matching circuit makes impedance substantially open load with respect to even number order higher harmonics of a fundamental wave of a high frequency signal.

According to a second aspect of the present invention, there is provided a high frequency power amplifier, comprising: a transistor for amplifying signals; and an input-side impedance matching circuit connected to an input side of the transistor, wherein the input-side impedance matching circuit makes impedance substantially short-circuit load with respect to odd number order higher harmonics of a fundamental wave of a high frequency signal.

According to a third aspect of the present invention, there is provided a high frequency power amplifier, comprising: a front stage transistor; a rear stage transistor; and an inter-stage impedance matching circuit connected between the front stage transistor and the rear stage transistor for matching impedances, wherein higher harmonics generated in the front stage transistor is inputted into the rear stage transistor, and a higher harmonic load of the rear stage transistor is adjusted by the inter-stage impedance matching circuit.

According to a fourth aspect of the present invention, there is provided a high frequency power amplifier comprising a transistor for amplifying signals divided into cell units that operate in parallel, wherein each cell unit comprises an input-side impedance matching circuit and an output-side impedance matching circuit, and each cell unit adjusts a higher harmonic load of a basic frequency viewed from a direction of the transistor.

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of the embodiments thereof taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a circuit configuration of a high frequency power amplifier in First Embodiment of the present invention.

Fig. 2 shows the result of measurement of change in the power load efficiencies (%) for the phase angles θ of 2nd and 3rd higher harmonics with

respect to the reflection coefficient Γ_{in} performed for the GaAs FET in First Embodiment of the present invention.

Fig. 3 shows a circuit configuration of a high frequency power amplifier in Second Embodiment of the present invention.

5 Fig. 4 shows a circuit configuration of a high frequency power amplifier in Third Embodiment of the present invention.

Fig. 5 shows loads on a Smith chart in Third Embodiment of the present invention.

10 Fig. 6 shows a circuit configuration of a high frequency power amplifier in Fourth Embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described below with
15 reference to the accompanying drawings. It is noted that the same reference symbols in the drawings denote the same or corresponding components.

According to the investigation based on simulations and experiments by the inventors of the present invention, it was confirmed that when the output-side higher harmonic conditions of an impedance matching circuit was
20 open load for even number order harmonics, and was short-circuit load for odd number order harmonics, higher efficiency could be achieved in a high frequency power amplifying circuit when the input-side 2nd (even number order) higher harmonic load of the impedance matching circuit was an open load or a high-impedance load. Furthermore, in the same case, it was confirmed that
25 higher efficiency could be achieved when the input-side 3rd (odd number order) higher harmonic load was a short-circuit load or a low-impedance load. In the following description, an example of the circuit configurations of the present invention for optimizing the input-side higher harmonic load of the impedance matching circuit for elevating the efficiency of transistor operation will be
30 described.

First Embodiment

Fig. 1 shows a circuit configuration of a high frequency power amplifier in First Embodiment of the present invention. In Fig. 1, reference numeral 1

denotes a transistor, 2 denotes a signal line 1 (line length: L1, line width: W1), 3 denotes a signal line 2 (line length: L2, line width: W2), 4 denotes a signal line 3 (line length: L3, line width: W3), 5 denotes a signal line 4 (line length: L4, line width: W4), 6 denotes a signal line 5 (line length: L5, line width: W5), 7 denotes an output-side matching circuit, 8 denotes a signal input terminal, and 9 denotes a signal output terminal. If impedance is not matched in the middle or ends of signal lines 1 or the like, a part of the incident wave is reflected. The ratio of this reflected wave to the incident wave is called a reflection coefficient. In Fig. 1, reference numeral 10 denotes the reflection coefficient (Γ_{in}) when the input-side matching circuit is viewed from the direction of the transistor 1. In general, the voltage $V(z)$ in the z -direction of the signal line that has a phase constant of β is represented by the following Equation 1.

[Equation 1]

$$V(z) = A \exp(-j\beta z) + B \exp(j\beta z) \quad (1)$$

where A and B are constants, the first term represents the incident wave, and the second term represents the reflected wave.

The ratio of the incident wave to the reflected wave, that is, the reflection coefficient $\Gamma(l)$ is represented by the following Equation 2.

[Equation 2]

$$\Gamma(l) = |B/A| \expj(2\beta l + \theta) \quad (2)$$

where $|B/A|$ represents the quantity of reflection, and θ represents the phase angle.

As Fig. 1 shows, signal lines 3, 4, and 5 are connected in series, the signal line 1 is connected to the node A between signal lines 3 and 4, and the signal line 2 is connected to the node B between signal lines 4 and 5. By adjusting line lengths $L1$ to $L5$ and line widths $W1$ to $W5$ of the signal lines 1 to 5 shown in Fig. 1, the 2nd higher harmonic is adjusted to be an open load (the reflected phase angle of Γ_{in} : $0 - 90^\circ$, the quantity of reflection: $0.6 - 1.0$), and the 3rd higher harmonic is adjusted to be short-circuit load (the reflected phase angle of Γ_{in} : $110 - 270^\circ$, the quantity of reflection: $0.6 - 1.0$).

Fig. 2 shows the result of measurement of change in the power load efficiencies (%) for the phase angles θ of 2nd and 3rd higher harmonics with respect to the reflection coefficient Γ_{in} performed for the GaAs FET in First Embodiment of the present invention. As Fig. 2 shows, the power load efficiency of the 2nd higher harmonic with respect to the phase angle θ of the reflection coefficient Γ_{in} is as high as 80% – 85% within the range of reflected phase angles $\theta = 0 - 90^\circ$, and is as low as 60% – 65% within the range of reflected phase angles $\theta = 130 - 190^\circ$. The power load efficiency of the 3rd higher harmonic with respect to the phase angle θ of the reflection coefficient Γ_{in} is as high as 80% – 85% within the range of reflected phase angles $\theta = 110 - 270^\circ$. Especially for the 3rd higher harmonic, it is known that there is the effect of inhibiting the lowering of efficiency within the range of reflected phase angles $\theta = 140 - 190^\circ$ by the 2nd higher harmonic (130 – 190°).

According to First Embodiment, as described above, by adjusting line lengths L1 to L5 and line widths W1 to W5 of the signal lines 1 to 5 in a high frequency power amplifying circuit shown in Fig. 1, the 2nd higher harmonic can be adjusted to be an open load (the reflected phase angle of Γ_{in} : $0 - 90^\circ$, the quantity of reflection: 0.6 – 1.0), and the 3rd higher harmonic is adjusted to be short-circuit load (the reflected phase angle of Γ_{in} : $110 - 270^\circ$, the quantity of reflection: 0.6 – 1.0). Therefore, by optimizing the input-side higher harmonic load of the impedance-matching circuit, the efficiency of transistor operation can be improved.

Second Embodiment

Fig. 3 shows a circuit configuration of a high frequency power amplifier in Second Embodiment of the present invention. In Fig. 3, since the same reference numerals as used in Fig. 1 denote the same elements, no description will be made for such elements. In Fig. 3, reference numeral 11 denotes an input-side fundamental wave matching circuit, 12 denotes an input-side 2nd higher harmonic processing circuit, and 13 denotes an input-side 3rd higher harmonic reflecting circuit. As Fig. 3 shows, the input-side fundamental wave matching circuit 11, the input-side 2nd higher harmonic processing circuit 12, and the input-side 3rd higher harmonic reflecting circuit 13 are connected in series. In order to improve the operation efficiency of the transistor 1 using the

higher harmonic processing circuit 12, the phase angle of reflection, as well as the quantity of reflection must be increased. In general, there is the problem that the higher the frequency of a signal, that is, the higher the order of higher harmonics, the smaller the amplitude of the higher harmonics reflected from the higher harmonic processing circuit 12 until the higher harmonics reach the input end of the transistor 1 due to propagation loss, and sufficient quantity of reflection cannot be obtained. However, as Fig. 3 shows, in the circuit configuration of the high frequency power amplifier in Second Embodiment of the present invention, the line length between the higher harmonic processing circuit 12 and the transistor 1 can be shortened, and the quantity of reflection of higher harmonics can be increased, by disposing the higher harmonic processing circuit 12 that processes the higher order higher harmonics closer to the transistor 1.

According to Second Embodiment, as described above, the line length between the higher harmonic processing circuit 12 and the transistor 1 can be shortened, and the quantity of reflection of higher harmonics can be increased, by disposing the higher harmonic processing circuit 12 that processes the higher order higher harmonics closer to the transistor 1.

Third Embodiment

Fig. 4 shows a circuit configuration of a high frequency power amplifier in Third Embodiment of the present invention. In Fig. 4, since the same reference numerals as used in Fig. 1 denote the same elements, no description will be made for such elements. In Fig. 4, reference numeral 14 denotes a front stage transistor, 15 denotes a rear stage transistor, 16 denotes an inter-stage matching circuit, 17 denotes an input-side reflection coefficient (Γ_{in} 1) viewed from the direction of the rear stage transistor 15, 18 denotes an output-side reflection coefficient (Γ_{out} 2) of the front stage transistor 14 viewed from the direction of the inter-stage matching circuit 16, and 19 denotes the reflection coefficient (Γ 2) of the front stage transistor 14 viewed from the direction of the inter-stage matching circuit 16.

As described above, higher harmonic loads are adjusted by reflection using a passive resonance circuit in the prior application. However, in Third Embodiment of the present invention, multiple stages of transistors are connected as Fig. 4 shows, and by inputting higher harmonics generated from the

front stage transistor 14 of the multiple-stage amplifier into the rear stage transistor 15, the higher harmonic loads of the rear stage transistor 15 can be controlled to be highly efficient without using a higher harmonic reflecting circuit utilizing a resonance circuit.

5 The object of Third Embodiment is to operate the rear stage transistor 15, which has a large output, in high efficiency, and to make the rear stage transistor 15 operate together with the front stage transistor 14 at the A to AB class operating point to generate more higher harmonic components. The inter-stage matching circuit 16 performs the inter-stage matching of the front stage
10 transistor 14 and the rear stage transistor 15, and matches their impedances for not only the fundamental wave but also higher harmonics to input higher harmonics generated in the front stage transistor 14 into the rear stage transistor 15. Since the load adjustment of the input-side higher harmonics of the rear stage transistor 15 is performed using higher harmonics actively
15 generated in the front stage transistor 14, a larger quantity of reflection can be obtained compared with the case where higher harmonics generated in the input side of the rear stage transistor 15 are reflected as in First Embodiment. The higher harmonic loads (phase, amplitude), when the inter-stage matching circuit 16 is viewed from the direction of the rear stage transistor 15, are adjusted so
20 that the efficiency of the rear stage transistor 15 becomes the maximum. Preferably, with respect to the reflection coefficient $\Gamma_{in 1}$ (17), the phase angle of the 3rd higher harmonic is $110 - 270^\circ$, and the quantity of reflection is $0.6 - 1.0$.

Furthermore, with respect to higher harmonics of even number or odd number orders, impedance matching is performed using the inter-stage matching
25 circuit 16 connected to the rear stage transistor 15 and to the front stage transistor 14. It is preferable that the high frequency generated from the front stage transistor 14 is inputted into the rear stage transistor 15, and the high-frequency load of the rear stage transistor 15 is adjusted as described above through the adjustment of the inter-stage matching circuit 16.

30 Fig. 5 shows loads on a Smith chart in Third Embodiment of the present invention. In Fig. 5, the reference numeral 20 denotes the input-side 2nd higher harmonic load ($Z_{in 1} (2 f_0)$) viewed from the direction of the rear stage transistor 15 of Fig. 4, 21 denotes the output-side 2nd higher harmonic load ($Z_{out 2} (2 f_0)$)

of the front stage transistor 14 viewed from the direction of the inter-stage matching circuit 16 of Fig. 4, and 22 denotes the 2nd higher harmonic load ($Z_{2(2f)}$) of the front stage transistor 14 viewed from the direction of the inter-stage matching circuit 16 of Fig. 4.

By the inter-stage matching circuit 16 of Fig. 4, the output-side 2nd higher harmonic load 21 of the front stage transistor 14 viewed from the direction of the inter-stage matching circuit 16, and the 2nd higher harmonic load 22 of the front stage transistor 14 viewed from the direction of the inter-stage matching circuit 16 are conjugated and matched; and the 2nd higher harmonic generated from the front stage transistor 14 is inputted into the rear stage transistor 15. Furthermore, by adjusting the line length of the inter-stage matching circuit 16 so as to match the load to the location of 17 in Fig. 4, highly efficient operation can be achieved.

According to Third Embodiment, as described above, the higher harmonic load of the rear stage transistor 15 can be controlled to be highly efficient without using a higher harmonic reflecting circuit utilizing a resonance circuit, by connecting multiple stages of transistors and inputting higher harmonics generated from the front stage transistor 14 of a multiple-stage amplifier into the rear stage transistor 15.

Fourth Embodiment

Fig. 6 shows a circuit configuration of a high frequency power amplifier in Fourth Embodiment of the present invention. In Fig. 6, since the same reference numerals as used in Figs. 1 or 3 denote the same elements, no description will be made for such elements. In Fig. 6, reference numeral 23 denotes an electric power distributing circuit, 24 denotes an electric power combining circuit, 25 denotes an output-side 3rd higher harmonic processing circuit, 26 denotes an output-side 2nd higher harmonic processing circuit, 27 denotes an output-side fundamental wave matching circuit, 28 denotes transistors divided into cell units, and 29 denotes the load of the input-side matching circuit (Z_{in}) viewed from the direction of transistors divided into cell units.

When the input/output load of a transistor lowers, the load of the input/output matching circuit for matching this lowers, and the quantity of

reflection of the fundamental wave increases. Therefore, the quantity of reflection of higher harmonics corresponding to the fundamental wave lowers. In Fourth Embodiment of the present invention, in order to increase the quantity of reflection of higher harmonics, transistors operating in parallel to the load of the fundamental wave are divided into cell units (28) to adjust the higher harmonic load of the input/output matching circuit 11 for each cell unit so as to be highly efficient. By combining units each containing a transistor cell 28 and an input/output matching circuit 11 in parallel using the electric power distributing circuit 23 and the electric power combining circuit 24 to increase the quantity of reflection of higher harmonics viewed from the direction of each transistor cell 28, the quantity of reflection of higher harmonics required for elevating the efficiency of the transistors 28 can be obtained. Since the variation of higher harmonic loads viewed from the direction of each transistor cell 28 can be minimized compared with the case where the higher harmonic processing circuit is formed without dividing the transistor, lowering of efficiency due to the uneven operation of each transistor can be prevented.

According to Fourth Embodiment, as described above, transistors operating in parallel to the load of the fundamental wave are divided into cell units to adjust the higher harmonic load of the input/output matching circuit 11 for each cell unit so as to be highly efficient. Therefore, since the variation of higher harmonic loads viewed from the direction of each transistor cell 28 can be minimized compared with the case where the higher harmonic processing circuit is formed without dividing any transistor, lowering of efficiency due to the uneven operation of each transistor can be prevented.

According to the high frequency power amplifier of the present invention, as described above, the efficiency of the operation of a transistor can be improved without limiting the input-side higher harmonic load of an impedance matching circuit to the short-circuit load, by optimizing the input-side higher harmonic load of the impedance matching circuit.

Furthermore, by disposing the higher harmonic processing circuit 12 of higher orders closer to the transistor 1, there is provided a high frequency power amplifier with the shortened line length between the higher harmonic processing

circuit 12 and the transistor 1, and increased quantity of reflection of higher harmonics.

In the high frequency power amplifier, a phase angle of reflection of a second higher harmonic may be 0 to 90 degrees, and a quantity of reflection may be 0.6 to 1.0, with respect to a reflection coefficient when the input-side impedance matching circuit is viewed from a direction of an input end of the transistor.

In the high frequency power amplifier, a phase angle of reflection of a third higher harmonic may be 110 to 270 degrees, and a quantity of reflection may be 0.6 to 1.0, with respect to a reflection coefficient when the input-side impedance matching circuit is viewed from a direction of an input end of the transistor.

In the high frequency power amplifier, the input-side impedance matching circuit may comprise a third higher harmonic reflecting circuit, a second higher harmonic processing circuit, and a fundamental wave matching circuit, disposed sequentially from a side of a signal input terminal.

The present invention has been described in detail with respect to various embodiments, and it will now be apparent from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the invention, therefore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

The entire disclosure of Japanese Patent Application No. 2000-362556 filed on November 29, 2000 including specification, claims, drawings and summary are incorporated herein by reference in its entirety.

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